

02-04-05

IFW / AF

PTO/SB/21 (09-04)

Approved for use through 7/31/2006
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction act of 1995, no persona are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

74

Application Number

09/698,497

Filing Date

October 27, 2000

First Named Inventor

Ahmadreza Rofougaran

Art Unit

2682

Examiner Name

Marceau Milord

Attorney Docket Number

15258US04

ENCLOSURES (check all that apply)

Fee Transmittal Form (1 Page)

Fee Attached (Check)

Amendment/Reply

After Final

Affidavits/declaration(s)

Extension of Time Request

Express Abandonment Request

Information Disclosure Statement

Certified Copy of Priority Document(s)

Reply to Missing Parts/ Incomplete Application

Reply to Missing Parts under 37 CFR 1.52 or 1.53

Drawing(s)

Licensing-related Papers

Petition

Petition to Convert to a Provisional Application

Power of Attorney, Revocation Change of Correspondence Address

Terminal Disclaimer

Request for Refund

CD Number of CD(s) _____

Landscape Table on CD

After Allowance Communication to TC

Appeal Communication to Board of Appeals and Interferences

Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)

Proprietary Information

Status Letter

Return-Receipt Postcard

Other Enclosure(s) (please identify below):

Remarks

Appeal Brief is enclosed in triplicate. Each Appeal Brief is 24 pages.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual Name

McAndrews Held & Malloy, Ltd.

Name (Print/type)

Michael T. Cruz

Registration No. (Attorney/Agent)

44,636

Signature

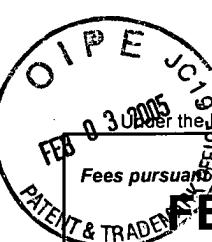
Michael T. Cruz

Date: February 3, 2005

EXPRESS MAIL DEPOSIT

U.S.P.S. Express Mail Mailing Label No. : EV 436 260 312 US.

Date of Deposit : February 3, 2005.



Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Effective on 12/08/2004.

Fees pursuant to the consolidated Appropriates Act. 2005 (H.R. 4818).

FEE TRANSMITTAL for FY 2005

Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT (\$)**500.00**

<i>Complete if Known</i>	
Application Number	09/698,497
Filing Date	October 27, 2000
First Named Inventor	Ahmadreza Rofougaran
Examiner Name	Marceau Milord
Art Unit	2682
Attorney Docket No.	15258US04

METHOD OF PAYMENT (check all that apply)

Check Credit Card Money Order None Other (please identify): _____

Deposit Account Deposit Account Number: 13-0017 Deposit Account Name: McAndrews Held & Malloy

For the above-identified deposit account, the Director is hereby authorized to (check all that apply)

- | | |
|--|---|
| <input type="checkbox"/> Charge Fee(s) indicated below | <input type="checkbox"/> Charge Fee(s) indicated below, except for the filing fee |
| <input checked="" type="checkbox"/> Charge any additional fee(s) or underpayments of fees(s) | <input type="checkbox"/> Credit any overpayments under 37 CFR 1.16 and 1.17 |

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid(\$)
	Fee (\$)	Small Entity Fee(\$)	Fee(\$)	Small Entity Fee(\$)	Fee(\$)	Small Entity Fee(\$)	
Utility	300	150	500	250	200	100	_____
Design	200	100	100	50	130	65	_____
Plant	200	100	300	150	160	80	_____
Reissue	300	150	500	250	600	300	_____
Provisional	200	100	0	0	0	0	_____

2. EXCESS CLAIM FEES

Fee Description

Each claim over 20, or for Reissues, each claim over 20 and more than in the original patent

Small Entity

Fee(\$) 50 25

Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent

Fee(\$) 200 100

Multiple dependent claims

Fee(\$) 360 180

Total Claims	Extra Claims	Fee(\$)	Fee Paid (\$)	Multiple Dependent Claims
-20 or HP	x	=		Fee Fee Paid (\$)

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee(\$)	Fee Paid (\$)	Multiple Dependent Claims
-3 or HP	x	=		Fee Fee Paid (\$)

HP = highest number of independent claims paid for, if greater than 3

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee(\$)	Fee Paid(\$)
-100	/50	(round up to a whole number)	x	=

4. OTHER FEE(S)

Non-English Specification, \$130 fee (no small entity discount)

Other: Filing a Brief in Support of an Appeal **500.00**

SUBMITTED BY

Signature	<i>Michael T. Cruz</i>	Registration No. (Attorney/Agent)	44,636	Telephone	(312) 775-8084
Name (print/type)	Michael T. Cruz		Date	February 3, 2005	



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Attorney Docket No. 15258US04

In the Application of:

Ahmadreza Rofougaran et al.

U.S. Serial No.: 09/698,497

Filed: October 27, 2000

For: ADAPTIVE RADIO TRANSCEIVER
WITH NOISE SUPPRESSION

Examiner: Marceau Milord

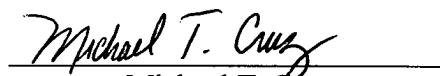
Group Art Unit: 2682

Confirmation No.: 3845

U.S.P.S. EXPRESS MAIL MAILING
LABEL NO. EV 436 260 312 US

Certificate of Express Mailing

I hereby certify that this correspondence is being deposited with the United States Postal Service as Express Mail in an envelope addressed to Mail Stop Appeal Brief - Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313 on February 3, 2005.



Michael T. Cruz
Reg. No. 44,636

APPEAL BRIEF

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a timely appeal from an Office Action Made Final mailed July 13, 2004, in which claims 1-26 were rejected.

02/07/2005 HDEMESS1 00000021 09698497

01 FC:1402

500.00 DP

REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California and having a place of business at 16215 Alton Parkway, Irvine, California 92618-3616, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment filed with the present application and recorded on Reel 012144, Frame 0484.

RELATED APPEALS AND INTERFERENCES

There are currently no appeals pending regarding related applications.

STATUS OF THE CLAIMS

Claims 1-26 are pending in the present application. Pending claims 1-26 have been rejected under 35 U.S.C. § 103(a) and are the subject of this appeal.

STATUS OF THE AMENDMENTS

There are no amendments pending in the present application.

SUMMARY OF THE INVENTION

Some embodiments according to some aspects of the present invention may provide a circuit that includes, for example, a logic circuit, a capacitor, a first resistor and a second resistor. The logic circuit may have, for example, a power input and a power return. The capacitor may be coupled, for example, across the power input and the power return. The first resistor may have, for example, a first end coupled to the power input and a second end to couple to a power source. The second resistor may have, for example, a first end coupled to the power return and a second end to couple to a power source return.

Some embodiment according to some aspects of the present invention may provide a circuit that includes, for example, logic means, charge means and isolation means. The logic means performs, for example, a logic function. The charge means

stores, for example, a charge across the logic means. The isolation means isolates, for example, the charge means from a power source.

Some embodiments according to some aspects of the present invention may provide a method of suppressing noise during the switching of a differential circuit having differential inputs and differential outputs. The method may include, for example, one or more of the following: charging a capacitor through a resistor, applying a signal transition at differential inputs, and circulating charge between the differential outputs through the capacitor.

Some embodiments according to some aspects of the present invention may provide an integrated circuit. The integrated circuit may include, for example, a differential circuit and an inductor. The differential circuit may have, for example, a power input. The inductor may have, for example, a first end coupled to the power input and a second end to couple to a power source.

Some embodiments according to some aspects of the present invention may provide a circuit that includes, for example, a differential circuit and a current source. The current source may have, for example, an output, an input and a capacitor. The output may be coupled, for example, to the differential circuit. The capacitor may shunt, for example, the input.

ISSUES FOR REVIEW

Whether claims 1-26 are unpatentable under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,983,082 to Mark F. Hilbert (“Hilbert”) in view of U.S. Patent No. 6,633,660 B1 to Karl H.T.J. Gardenfors et al. (“Gardenfors”).

GROUPING OF CLAIMS

Claims 1-26 do not stand or fall together.

Group I. Claims 1-7 stand or fall together.

Group II. Claims 8-10, 12, 13 and 15 stand or fall together.

Group III. Claims 11 and 14 stand or fall together.

Group IV. Claim 16 stands or falls by itself.

- Group V. Claims 17 and 18 stand or fall together.
- Group VI. Claim 19 stands or falls by itself.
- Group VII. Claim 20 stands or falls by itself.
- Group VIII. Claim 21 stands or falls by itself.
- Group IX. Claim 22 stands or falls by itself.
- Group X. Claims 23-26 stand or fall together.

ARGUMENT

I. Group I: Claims 1-7

Claims 1-7 stand rejected under 35 U.S.C. § 103(a) as being obvious over Hilbert in view of Gardenfors.

Claim 1 is reproduced below.

1. A circuit, comprising:
 a logic circuit having a power input and a power return;
 a capacitor coupled across the power input and the power return;
 a first resistor having a first end coupled to the power input and a second end to couple to a power source; and
 a second resistor having a first end coupled to the power return and a second end to couple to a power source return.

To maintain an obviousness rejection, each and every element as set forth in claim 1 must be taught or suggested by Hilbert in view of Gardenfors. Appellants respectfully submit that each and every element as set forth in claim 1 is not taught or suggested by Hilbert in view of Gardenfors.

In the Office Action mailed July 13, 2004 ("the Final Office Action"), the Examiner stated that

Hilbert does not specifically disclose a capacitor coupled across the power input and the power return; and a first resistor having a first end coupled to the power input and a second end to couple to a power source.

The Final Office Action at page 2.

Appellants agree with the Examiner that Hilbert does not teach or suggest at least these elements. Appellants respectfully note that, in the Final Office Action, the Examiner did not explain how Gardenfors teaches the elements that Hilbert does not

teach such as, for example, a capacitor coupled across a power input and a power return; and a first resistor having a first end coupled to the power input and a second end to couple to a power source. Appellants respectfully submit that the Final Office Action is silent as to how Gardenfors or Hilbert teaches a power input, a power return, a power source and a power source return as set forth in claim 1. Furthermore, the Final Office Action is silent as to how Gardenfors or Hilbert teaches the power input, the power return, the power source, the power source return and their interrelationships with the other recited elements as set forth in claim 1.

In the Advisory Action mailed November 5, 2004 (“the Advisory Action”), the Examiner proposed the following argument with regard to claim 1 and the other claims: Gardenfors teaches a radio transceiver integrated into one integrated circuit (IC) chip. According to the Examiner, since Gardenfors teaches integration on a single IC chip, “all the components are implemented into the single integrated circuit (resistors, capacitors, transistors, etc)”. The Advisory Action at page 2. In other words, it is the Examiner’s assertion, that by merely mentioning a single IC chip, Gardenfors must teach most, if not all, of the individual elements recited in the claims and thus, the “Examiner still believes that Hilbert and Gardenfors teach all the claimed limitations”. The Advisory Action at page 2. Appellants respectfully submit that the Examiner’s assertion is erroneous. Just because Gardenfors mentions a single IC chip does not mean Gardenfors teaches at least the elements not taught by Hilbert. For example, in the Advisory Action, the Examiner asserts that, because Gardenfors mentions a single IC chip, Gardenfors must therefore teach resistors and capacitors despite the fact that the figures of Gardenfors show no resistors and capacitors and the specification of Gardenfors is silent as to resistors and capacitors. However, the Examiner’s assertion must be stretched even further. Despite Gardenfors not specifically mentioning a resistor, a capacitor, a power input, a power source, a power return, a power source return and the Examiner not pointing, with any particularity, to a resistor, a capacitor, a power input, a power source, a power return, a power source return in Gardenfors, the Examiner nevertheless alleges that Gardenfors also somehow teaches a first resistor, a second resistor, a capacitor and their recited interrelationships with a power input, a power source, a power return and a power source

return as set forth in claim 1. Appellants respectfully submit that neither Gardenfors nor Hilbert, individually or combined, support the Examiner's assertions.

Appellants respectfully submit that not even a *prima facie* case of obviousness has not been presented. See, e.g., M.P.E.P. § 2142 ("[t]he examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not produce a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness"). Appellants respectfully submit that the Examiner has still not identified the power input, the power return, the power source and the power source return. Appellants further submit respectfully that, even if the Examiner has identified the power input, the power return, the power source and the power source return, the Examiner has not justified the interrelationship between the power input, the power return, the power source and the power source return with, for example, the capacitor, the first resistor and the second resistor as set forth in claim 1. Appellants again respectfully note that Gardenfors does not even mention a capacitor nor a resistor. Gardenfors is silent as to a power input, a power return, a power source and a power source return. Appellants respectfully submit Gardenfors does not teach or suggest "a capacitor coupled across the power input and the power return; a first resistor having a first end coupled to the power input and the a second end to couple to a power source; and a second resistor having a first end coupled to the power return and a second end to coupled to a power source return". Accordingly, Appellants respectfully submit that Gardenfors and Hilbert, individually or combined, do not teach or suggest each and every element including their interrelationships as recited in claim 1.

Appellants respectfully submit that claim 1 and its dependent claims (i.e., claims 2-7) are patentable over Hilbert in view of Gardenfors.

II. Group II: Claim 8-10, 12, 13 and 15

Claims 8-10, 12, 13 and 15 stand rejected under 35 U.S.C. § 103(a) as being obvious over Hilbert in view of Gardenfors.

Claim 8 is reproduced below.

8. A circuit, comprising:
logic means for performing a logic function;
charge means for storing a charge across the logic means; and

isolation means for isolating the charge means from a power source.

To maintain an obviousness rejection, each and every element as set forth in claim 1 must be taught or suggested by Hilbert in view of Gardenfors. Appellants respectfully submit that each and every element as set forth in claim 8 is not taught or suggested by Hilbert in view of Gardenfors. For example, neither Hilbert nor Gardenfors, individually or combined, teach or suggest isolation means for isolating the charge means from a power source.

The Examiner has admitted that

Hilbert does not specifically disclose an isolation means for isolating the charge means from a power source.

The Final Office Action at page 4.

Accordingly, the Examiner must presumably allege that Gardenfors teaches isolation means for isolating the charge means from a power source. However, the discussion presented by the Examiner with respect to Gardenfors does not even mention isolation means. See, e.g., the Final Office Action at page 4.

Appellants respectfully draw the attention of the Board to the fact that the explanation on page 4 of the Final Office Action as to how Gardenfors teaches “isolation means for isolating the charge means from a power source” with respect to claim 8 is the *exact same explanation* as the explanation on pages 2 and 3 of the Final Office Action as to how Gardenfors allegedly taught “a capacitor coupled across the power input and the power return; and a first resistor having a first end coupled to the power input and a second end to coupled to a power source” with respect to claim 1. Once again, the explanation with respect to Gardenfors is silent as to how Gardenfors makes up for the admitted teaching deficiencies of Hilbert.

Appellants respectfully submit that Gardenfors does not even mention isolating charge means and does not mention isolating charge means from a power source. The Examiner did describe a phase locked loop, but does not explain any relationship between the phase locked loop and isolating charge means from a power source. If the Examiner did not discuss how Gardenfors teaches isolation means for isolating the charge means from a power source and Gardenfors, itself, does not even mention isolation means for isolating charge means from a power source, then Appellants respectfully disagree that

Gardenfors makes up for the admitted teaching deficiencies of Hilbert and that the combination of Hilbert and Gardenfors teaches isolation means for isolating the charge means from a power source. Appellants respectfully submit that the Examiner has not presented even a *prima facie* case of obviousness.

Although isolating charge means from a power source was not specifically mentioned in the Advisory Action, Appellants respectfully must disagree that with any possible assertion that, just because Gardenfors mentions a single IC chip, it must therefore teach isolating charge means from a power source.

Appellants respectfully submit that the Examiner has not even presented a *prima facie* case of obviousness. Furthermore, Appellants respectfully submit that, since Gardenfors does not mention isolating charge, Gardenfors does not teach isolating charge means from a power source. Thus, Appellants respectfully submit that Gardenfors does not make up for the admitted deficiencies of Hilbert.

Appellants respectfully submit that claim 8 and its dependent claims in the group (i.e., claims 9, 10, 12, 13 and 15) are patentable over Hilbert in view of Gardenfors.

III. Group III: Claims 11 and 14

Claims 11 and 14 stand rejected under 35 U.S.C. § 103(a) as being obvious over Hilbert in view of Gardenfors.

Since claims 11 and 14 depend directly or indirectly from claim 8, Appellants respectfully submit that claims 11 and 14 are patentable over Hilbert in view of Gardenfors for the reasons stated with respect to claim 8.

To maintain an obviousness rejection, each and every element as set forth in claim 11 must be taught or suggested by Hilbert in view of Gardenfors. Appellants respectfully submit that each and every element as set forth in claim 11 is not taught or suggested by Hilbert in view of Gardenfors.

Claim 11, which indirectly depends from claim 8, is reproduced below.

11. The circuit of claim 8 wherein the logic means comprises a differential circuit.

With respect to claim 8, the Examiner has already alleged that Hilbert and Gardenfors teach logic means by Hilbert teaching a variable current controller 809 of

FIG. 8. The Final Office Action at page 3. Appellants respectfully submit that the variable current controller 809 in FIG. 8 of Hilbert does not comprise a differential circuit. Instead of a differential circuit configuration, Hilbert teaches that NPN transistors 810-812 be arranged in a current mirror configuration. Appellant respectfully draw the attention of the Board to how the bases of the three transistors are connected and how the middle transistor is in a diode configuration. This is a current mirror configuration, not a differential circuit as alleged by the Examiner. The Examiner need only attempt to identify the differential inputs of the variable current controller 809 of Hilbert to understand that the variable current controller 809 is not a differential circuit. Furthermore, Gardenfors is silent as to a variable current controller using a differential circuit. Even if Gardenfors did teach differential circuits, Appellants respectfully submit that there is no teaching to modify the variable current controller of Hilbert to use differential circuits instead of or in addition to the above-described current mirror configuration.

For at least the above reasons, Appellants respectfully submit that claim 11 and its dependent claim in the group (i.e., claim 14) are patentable over Hilbert in view of Gardenfors.

IV. Group IV: Claim 16

Claim 16 stands rejected under 35 U.S.C. § 103(a) as being obvious over Hilbert in view of Gardenfors.

Claim 16, which depends indirectly from claim 8, is reproduced below.

16. The circuit of claim 15 wherein the CMOS inverters each comprises a p-channel transistor having a source coupled to the first end of the capacitor, a gate, and a drain, and an n-channel transistor having a source coupled to the second end of the capacitor, a gate coupled to the gate of the p-channel transistor to form an input node, and a drain coupled to the drain of the p-channel transistor to form an output node, the differential circuit further having a differential input comprising the input nodes for each of the CMOS inverters, and a differential output comprising the output nodes for each of the CMOS inverters.

Since claim 16 indirectly depends from claim 8, Appellants respectfully submit that claim 16 is patentable over Hilbert in view of Gardenfors for the reasons stated with respect to claim 8.

Since claim 16 indirectly depends from claim 11, Appellants respectfully submit that claim 16 is patentable over Hilbert in view of Gardenfors for the reasons stated with respect to claim 11.

To maintain an obviousness rejection, each and every element as set forth in claim 1 must be taught or suggested by Hilbert in view of Gardenfors. Appellants respectfully submit that each and every element as set forth in claim 16 is not taught or suggested by Hilbert in view of Gardenfors.

Claim 16 depends from claim 15 which depends from claim 14 which depends from claim 13 which depends from 12 which depends from claim 11 which depends from claim 8. Thus, the CMOS inverters recited in claim 15 are part of the two logic gates of claim 15 which are part of the differential circuit of claim 12 which is part of the logic means of claim 11 which depends from claim 8. For logical consistency, the Examiner needed to use the same element for logic means in claim 8 as is used in claim 16 since claim 16 indirectly depends from claim 8. The Examiner did not do this. The CMOS inverters must be a subset of the variable current controller 809 of FIG. 8 of Hilbert as alleged by the Examiner since, in claim 8, the Examiner alleged that the logic means was merely the variable current controller 809 of FIG. 8 of Hilbert. See the Final Office Action at page 3. The Examiner cannot now in a dependent claim use the inconsistent and different interpretation that the logic means is the variable phase shift network 420 as alleged by the Examiner with respect to claim 16. The Final Office Action at page 3. The variable phase shift network 420 is not a subset of the variable current controller 809. Accordingly, Appellants respectfully submit that the Examiner has provided an argument that logically cannot be maintained. Neither Hilbert nor Gardenfors, individually or combined, teaches a variable current controller 809 that includes, for example, CMOS inverters, an n-channel transistor and a p-channel transistor, and a differential circuit as set forth in claim 16. Even if Hilbert and Gardenfors teach CMOS inverters, an n-channel transistor, a p-channel transistor and a differential circuit, Hilbert and Gardenfors do not teach modifying the variable current controller 809 of Hilbert to include such

elements and certainly do not teach the interrelationships between the elements as set forth in claim 16.

For at least the above reasons, Appellants respectfully submit that claim 16 is patentable over Hilbert in view of Gardenfors.

V. Group V: Claims 17 and 18

Claims 17 and 18 stand rejected under 35 U.S.C. § 103(a) as being obvious over Hilbert in view of Gardenfors.

Claim 17 is reproduced below.

17. A method of suppressing noise during the switching of a differential circuit having differential inputs and differential outputs, comprising:

charging a capacitor through a resistor;
applying a signal transition at the differential inputs; and
circulating charge between the differential outputs through the capacitor.

To maintain an obviousness rejection, each and every element as set forth in claim 17 must be taught or suggested by Hilbert in view of Gardenfors. Appellants respectfully submit that each and every element as set forth in claim 17 is not taught or suggested by Hilbert in view of Gardenfors. For example, neither Hilbert nor Gardenfors, individually or combined, teach or suggest circulating charge between the differential outputs through the capacitor.

The Examiner has admitted that

Hilbert does not specifically disclose the features of circulating charge between the differential outputs through the capacitor; compensating for loss of the charge on the capacitor during the circulation of charge by recharging the capacitor through the resistor.

The Final Office Action at page 5.

Accordingly, the Examiner must allege that Gardenfors teaches, for example, circulating charge between the differential outputs through the capacitor. However, the discussion presented by the Examiner with respect to Gardenfors does not even mention circulating charge. See, e.g., the Final Office Action at pages 5 and 6.

Appellants respectfully draw the attention of the Board to the fact that the explanation on pages 5 and 6 of the Final Office Action as to how Gardenfors teaches “circulating charge between the differential outputs through the capacitor” with respect to

claim 17 and “compensating for loss of the charge on the capacitor during the circulation of charge by recharging the capacitor through the resistor” with respect to claim 18 is the *exact same explanation* as the explanation on page 4 of the Final Office Action as to how Gardenfors allegedly taught “isolation means for isolating the charge means from a power source” with respect to claim 8; and the explanation on pages 2 and 3 of the Final Office Action as to how Gardenfors allegedly taught “a capacitor coupled across the power input and the power return; and a first resistor having a first end coupled to the power input and a second end to coupled to a power source” with respect to claim 1. Once again, the explanation with respect to Gardenfors is silent as to how Gardenfors makes up for the admitted teaching deficiencies of Hilbert. Since the Examiner did not discuss how Gardenfors teaches circulating charge between differential outputs through a capacitor and Gardenfors, itself, does not even mention circulating charge through a capacitor, then Appellants respectfully submit that the combination of Hilbert and Gardenfors does not teach circulating charge between differential outputs through a capacitor. It is respectfully submitted that the Examiner has not presented even a *prima facie* case of obviousness.

In the Advisory Action, the Examiner does not address the issues raised with respect to claim 17. There is no mention or discussion of circulating charge between the differential outputs through a capacitor as set forth in claim 17. Appellants respectfully submit that, by merely mentioning a single IC chip, Gardenfors does not teach circulating charge between the differential outputs through a capacitor. In fact, Gardenfors does not even mention capacitors at all.

Neither Hilbert nor Gardenfors, individually or combined, teaches or suggests a method of suppressing noise during the switching of a differential circuit having differential inputs and outputs as set forth in claim 17. The Examiner alleged that a method of suppressing noise during the switching of a differential circuit is illustrated in FIGS. 3 and 8 of Hilbert. Although Hilbert and Gardenfors might possibly comment on noise reduction generally, Hilbert and Gardenfors do not teach or suggest suppressing noise during the switching of a differential circuit. Thus, even if the Examiner could allege that Hilbert and Gardenfors teach charging, applying and circulating as set forth in claim 17, the Examiner has not provided any evidence that the acts are part of a method

for suppressing noise *during the switching of a differential circuit*. Furthermore, Appellants respectfully submit that, by merely mentioning a single IC chip, Gardenfors or Hilbert in view of Gardenfors does not teach a method for suppressing noise during the switching of a differential circuit.

For at least the above reasons, Appellants respectfully submit that claim 17 and its dependent claim in the group (i.e., claim 18) are patentable over Hilbert in view of Gardenfors.

VI. Group VI: Claim 19

Claim 19 stands rejected under 35 U.S.C. § 103(a) as being obvious over Hilbert in view of Gardenfors.

Since claim 19 depends indirectly from claim 8, Appellants respectfully submit that claim 19 is patentable over Hilbert in view of Gardenfors for the reasons stated with respect to claim 17.

Claim 19, which depends from claim 18 which, in turn, depends from claim 17, is reproduced below.

19. The method of claim 18 further comprising clocking the differential circuit after a transition of the signal at the differential output, the circulation of the charge being initiated by clocking the differential circuit, the resistor and capacitor having a time constant that is less than half the clocking frequency.

To maintain an obviousness rejection, each and every element as set forth in claim 19 must be taught or suggested by Hilbert in view of Gardenfors. Appellants respectfully submit that each and every element as set forth in claim 19 is not taught or suggested by Hilbert in view of Gardenfors. For example, the Examiner alleges that col. 7, line 28 to col. 8, line 67 of Hilbert teaches each and every one of these elements of the dependent claim 19. See the Final Office Action at page 6. Although Hilbert teaches inputting a differential clock signal into signal inputs $V(0^\circ)$ and $V(180^\circ)$ to produce two sets of outputs $X(0^\circ)$ and $X(180^\circ)$ and $Y(0^\circ)$ and $Y(180^\circ)$, nowhere does Hilbert nor Gardenfors teach clocking a differential circuit after a transition of the signal at the differential output. Furthermore, Hilbert and Gardenfors do not teach initiating the circulation of charge by clocking the differential circuit. Finally, Hilbert and Gardenfors do not teach a

resistor and capacitor in the context of claim 19, which depends from claims 18 which depends from claim 17, in which the resistor and the capacitor have a time constant that is less than half the clocking frequency. In fact, neither Hilbert nor Gardenfors even mentions time constants.

For at least the above reasons, Appellants respectfully submit that claim 19 is patentable over Hilbert in view of Gardenfors.

VII. Group VII: Claim 20

Claim 20 stands rejected under 35 U.S.C. § 103(a) as being obvious over Hilbert in view of Gardenfors.

Claim 20 is reproduced below.

20. An integrated circuit, comprising:
a differential circuit having a power input; and
an inductor having a first end coupled to the power input and a second end to couple to a power source.

To maintain an obviousness rejection, each and every element as set forth in claim 20 must be taught or suggested by Hilbert in view of Gardenfors. Appellants respectfully submit that each and every element as set forth in claim 20 is not taught or suggested by Hilbert in view of Gardenfors. For example, neither Hilbert nor Gardenfors, individually or combined, teaches or suggests an inductor having a first end coupled to the power input and a second end to couple to a power source.

The Examiner has admitted that

Hilbert does not specifically disclose an inductor having a first end coupled to the power input and a second end to couple to a power source; and a second inductor having a first end coupled to the power return and a second end to couple to a power source return.

The Final Office Action at page 6.

Accordingly, the Examiner must allege that Gardenfors teaches, for example, an inductor having a first end coupled to the power input and a second end to couple to a power source.

Appellants respectfully draw the attention of the Board to the fact that the explanation on pages 6 and 7 of the Final Office Action as to how Gardenfors teaches “an

inductor having a first end coupled to the power input and a second end to couple to a power source” with respect to claim 20 is the exact same explanation as the explanations: on pages 5 and 6 of the Final Office Action as to how Gardenfors teaches “circulating charge between the differential outputs through the capacitor” with respect to claim 17 and “compensating for loss of the charge on the capacitor during the circulation of charge by recharging the capacitor through the resistor” with respect to claim 18; on page 4 of the Final Office Action as to how Gardenfors allegedly taught “isolation means for isolating the charge means from a power source” with respect to claim 8; on pages 2 and 3 of the Final Office Action as to how Gardenfors allegedly taught “a capacitor coupled across the power input and the power return; and a first resistor having a first end coupled to the power input and a second end to couple to a power source” with respect to claim 1. Once again, the explanation with respect to Gardenfors is silent as to how Gardenfors makes up for the admitted teaching deficiencies of Hilbert. Since the Examiner did not discuss how Gardenfors teaches an inductor having a first end coupled to the power input and a second end to couple to a power source and Gardenfors, itself, does not appear to teach an inductor coupled to a differential circuit and a power source, Appellants respectfully submit that the Examiner has not presented even a *prima facie* case of obviousness. Appellants respectfully submit that the combination of Hilbert and Gardenfors does not teach at least these elements.

Even if Gardenfors did teach an inductor because, by merely mentioning a single IC chip, Gardenfors teaches an inductor as possibly alleged by the Examiner, neither Hilbert nor Gardenfors, individually or combined, teaches or suggests an inductor having a first end coupled to a power input of a differential circuit and a second end to couple to a power source.

For at least the above reasons, Appellants respectfully submit that claim 20 is patentable over Hilbert in view of Gardenfors.

VIII. Group VIII: Claim 21

Claim 21 stands rejected under 35 U.S.C. § 103(a) as being obvious over Hilbert in view of Gardenfors.

Since claim 21 depends from claim 20, Appellants respectfully submit that claim 21 is patentable over Hilbert in view of Gardenfors for the reasons stated with respect to claim 20.

Claim 21 is reproduced below.

21. The integrated circuit of claim 20 wherein the differential circuit further comprises a power return, the integrated circuit further comprising a second inductor having a first end coupled to the power return and a second end to couple to a power source return.

To summarize some elements of claims 20 and 21, a differential circuit comprises a power input and a power return. A first inductor has a first end coupled to the power input and a second end to couple to a power source. A second inductor has a first end coupled to the power return and a second end to couple to a power source return.

To maintain an obviousness rejection, each and every element as set forth in claim 21 must be taught or suggested by Hilbert in view of Gardenfors. Appellants respectfully submit that each and every element as set forth in claim 21 is not taught or suggested by Hilbert in view of Gardenfors. For example, neither Hilbert nor Gardenfors, individually or combined, teach or suggest a second inductor having a first end coupled to the power return and a second end to couple to a power source return.

The Examiner has admitted that

Hilbert does not specifically disclose an inductor having a first end coupled to the power input and a second end to couple to a power source; and a second inductor having a first end coupled to the power return and a second end to couple to a power source return.

The Final Office Action at page 6.

Accordingly, the Examiner must presumably allege that Gardenfors teaches, for example, an inductor having a first end coupled to the power input and a second end to couple to a power source and a second inductor having a first end coupled to the power return and a second end to couple to a power source return.

However, the explanation, which was provided by the Examiner as to how Gardenfors makes up for the teaching deficiencies of Hilbert, does not even mention inductors and, in particular, an inductor having a first end coupled to the power input and a second end to couple to a power source and a second inductor having a first end

coupled to the power return and a second end to couple to a power source return. See the Final Office Action at pages 6 and 7. The explanation is further deficient in explaining how Gardenfors teaches a power input, a power return, a power source and a power source return. Appellants respectfully submit that the Examiner has not presented even a *prima facie* case of obviousness.

In the Advisory Action, the Examiner presumably made the argument that, because Gardenfors mentions a single IC chip, Gardenfors teaches all of the individual elements as set forth in dependent claim 21 and its corresponding independent claim 20. Appellants respectfully submit that the Examiner's assertion is erroneous. Just because Gardenfors mentions a single IC chip does not mean that Gardenfors teaches, without any support in Gardenfors, an inductor, a second inductor, a differential circuit, a power input, a power return, a power source and a power source return. Even if Gardenfors did teach these elements, neither Gardenfors nor Hilbert, individually or combined, teaches the interrelationships between the elements as set forth in dependent claim 21 and its corresponding independent claim 20.

For at least the above reasons, Appellants respectfully submit that claim 21 is patentable over Hilbert in view of Gardenfors.

IX. Group IX: Claim 22

Claim 22 stands rejected under 35 U.S.C. § 103(a) as being obvious over Hilbert in view of Gardenfors.

Since claim 22 depends from claim 20, Appellants respectfully submit that claim 22 is patentable over Hilbert in view of Gardenfors for the reasons stated with respect to claim 20.

Claim 22 is reproduced below.

22. The integrated circuit of claim 20 wherein the inductor comprises a spiral inductor.

To maintain an obviousness rejection, each and every element as set forth in claim 22 must be taught or suggested by Hilbert in view of Gardenfors. Appellants respectfully submit that each and every element as set forth in claim 22 is not taught or suggested by Hilbert in view of Gardenfors. For example, neither Hilbert nor Gardenfors, individually

or combined, teach or suggest a second inductor having an inductor as set forth in claim 20 that comprises a spiral inductor. The Examiner does not even discuss a spiral inductor either in the Final Office Action or in the Advisory Action. See the Final Office Action at pages 6 and 7; the Advisory Action at page 2. Neither Hilbert nor Gardenfors mentions a spiral inductor. Appellants respectfully submit that the Examiner has not presented even a *prima facie* case of obviousness. Appellants respectfully submit that neither Hilbert nor Gardenfors, individually or combined, teaches a spiral inductor.

Appellants respectfully submit that, just because Gardenfors mentions a single IC chip as alleged by the Examiner, Gardenfors does not teach a spiral inductor. Even if Gardenfors did teach a spiral inductor, neither Gardenfors nor Hilbert, individually or combined, teaches a spiral inductor as set forth in dependent claim 22 in view of claim 20.

For at least the above reasons, Appellants respectfully submit that claim 22 is patentable over Hilbert in view of Gardenfors.

X. Group X: Claims 23-26

Claims 23-26 stand rejected under 35 U.S.C. § 103(a) as being obvious over Hilbert in view of Gardenfors.

Claim 23 is reproduced below.

23. A circuit, comprising:
 - a differential circuit; and
 - a current source having an output coupled to the differential circuit, an input, and a capacitor shunting the input.

To maintain an obviousness rejection, each and every element as set forth in claim 23 must be taught or suggested by Hilbert in view of Gardenfors. Appellants respectfully submit that each and every element as set forth in claim 23 is not taught or suggested by Hilbert in view of Gardenfors. For example, neither Hilbert nor Gardenfors, individually or combined, teach or suggest a current source having an output coupled to a differential circuit, an input, and a capacitor shunting the input.

The Examiner has admitted that

Hilbert does not specifically disclose a current source having an output coupled to the differential circuit, an input, and a capacitor shunting the input.

The Final Office Action at page 7.

Accordingly, the Examiner must allege that Gardenfors teaches a current source having an output coupled to a differential circuit, an input, and a capacitor shunting the input. However, the discussion presented by the Examiner with respect to Gardenfors does not even mention a current source, a differential circuit, a capacitor. See the Final Office Action at pages 7 and 8. Instead, the Examiner again used the exact same explanation as to how Gardenfors made up for the teaching deficiencies of Hilbert that was used in the rejection of the other independent claims (i.e., claim 1, 8, 17 and 20). And again, the explanation of Gardenfors did not discuss the elements of the claim that were admitted to be the teaching deficiencies of Hilbert. Appellants respectfully submit that the Examiner has not presented even a *prima facie* case of obviousness.

Presumably, the Examiner in the Advisory Action again made the same argument with respect to claim 23, namely, that, because Gardenfors mentions a single IC chip, Gardenfors teaches all of the individual components recited in the all of the claims. As has been argued many times previously, just because Gardenfors may have mentioned a single IC chip does not mean Gardenfors teaches a current source, a differential circuit and a capacitor. Furthermore, even if Gardenfors did teach a current source, a differential circuit and a capacitor, neither Hilbert nor Gardenfors, individually or combined teaches or suggests the interrelationships between the elements as set forth in claim 23. For example, neither Hilbert nor Gardenfors, individually or combined, teaches or suggests a capacitor shunting an input of a current source that is coupled to a differential circuit. In fact, Appellants respectfully submit that Gardenfors does not even mention a capacitor anywhere. If the Examiner did not discuss how Gardenfors teaches a capacitor shunting an input of a current source that is coupled to a differential circuit and Gardenfors, itself, does not even mention a capacitor, then Appellants must respectfully submit that the combination of Hilbert and Gardenfors does not teach or suggest, for example, a capacitor shunting an input of a current source that is coupled to a differential circuit as set forth in claim 23.

For at least the above reasons, Appellants respectfully submit that claim 23 and its dependent claims (i.e., claims 24-26) are patentable over Hilbert in view of Gardenfors.

XI. Conclusion

For the foregoing reasons, claims 1-26 are distinguishable over the prior art of record. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: February 3, 2005

Respectfully submitted,



Michael T. Cruz
Registration No. 44,636
Attorney for Appellants

McANDREWS, HELD & MALLOY, LTD.
500 West Madison Street, 34th Floor
Chicago, Illinois 60661-2565
Telephone: (312) 775-8084
Facsimile: (312) 775-8100

APPENDIX

The following claims are involved in this appeal:

1. A circuit, comprising:
 - a logic circuit having a power input and a power return;
 - a capacitor coupled across the power input and the power return;
 - a first resistor having a first end coupled to the power input and a second end to couple to a power source; and
 - a second resistor having a first end coupled to the power return and a second end to couple to a power source return.
2. The circuit of claim 1 wherein the logic circuit comprises a differential circuit.
3. The circuit of claim 2 wherein the differential circuit comprises two logic gates.
4. The circuit of claim 3 wherein the two logic gates are the same type of gate.
5. The circuit of claim 4 wherein the two logic gates each comprises an inverter.
6. The circuit of claim 5 wherein the two logic gates each further comprises complementary metal oxide semiconductor (CMOS) inverters.
7. The circuit of claim 6 wherein the CMOS inverters each comprises a p-channel transistor having a source coupled to the power input, a gate, and a drain, and an n-channel transistor having a source coupled to the power return, a gate coupled to the gate of the p-channel transistor to form an input node, and a drain coupled to the drain of

the p-channel transistor to form an output node, the differential circuit further having a differential input comprising the input nodes for each of the CMOS inverters, and a differential output comprising the output nodes for each of the CMOS inverters.

8. A circuit, comprising:

logic means for performing a logic function;

charge means for storing a charge across the logic means; and

isolation means for isolating the charge means from a power source.

9. The circuit of claim 8 wherein the charge means comprises a capacitor.

10. The circuit of claim 9 wherein the isolation means comprises a first resistor to couple a first end of the capacitor to the power source, and a second resistor to couple a second end of the capacitor to a return line for the power source.

11. The circuit of claim 8 wherein the logic means comprises a differential circuit.

12. The circuit of claim 11 wherein the differential circuit comprises two logic gates.

13. The circuit of claim 12 wherein the two logic gates are the same type of gate.

14. The circuit of claim 13 wherein the two logic gates each comprises an inverter.

15. The circuit of claim 14 wherein the two logic gates each further comprises complementary metal oxide semiconductor (CMOS) inverters.

16. The circuit of claim 15 wherein the CMOS inverters each comprises a p-channel transistor having a source coupled to the first end of the capacitor, a gate, and a drain, and an n-channel transistor having a source coupled to the second end of the capacitor, a gate coupled to the gate of the p-channel transistor to form an input node, and a drain coupled to the drain of the p-channel transistor to form an output node, the differential circuit further having a differential input comprising the input nodes for each of the CMOS inverters, and a differential output comprising the output nodes for each of the CMOS inverters.

17. A method of suppressing noise during the switching of a differential circuit having differential inputs and differential outputs, comprising:

- charging a capacitor through a resistor;
- applying a signal transition at the differential inputs; and
- circulating charge between the differential outputs through the capacitor.

18. The method of claim 17 further comprising compensating for loss of the charge on the capacitor during the circulation of charge by recharging the capacitor through the resistor.

19. The method of claim 18 further comprising clocking the differential circuit after a transition of the signal at the differential output, the circulation of the charge being initiated by clocking the differential circuit, the resistor and capacitor having a time constant that is less than half the clocking frequency.

20. An integrated circuit, comprising:
a differential circuit having a power input; and
an inductor having a first end coupled to the power input and a second end to couple to a power source.

21. The integrated circuit of claim 20 wherein the differential circuit further comprises a power return, the integrated circuit further comprising a second inductor

having a first end coupled to the power return and a second end to couple to a power source return.

22. The integrated circuit of claim 20 wherein the inductor comprises a spiral inductor.

23. A circuit, comprising:
a differential circuit; and
a current source having an output coupled to the differential circuit, an input, and
a capacitor shunting the input.

24. The circuit of claim 23 wherein the current source comprises a transistor having a drain coupled to the differential circuit, a gate and a source, the capacitor being coupled between the gate and the source.

25. The circuit of claim 24 further comprising a bias circuit coupled to the gate of the transistor.

26. The circuit of claim 25 wherein the bias circuit comprises a resistor.